1 July 2018

Fabless silicon photonics operation and design trends

LETI INNOVATION DAYS 2018

Silicon photonics

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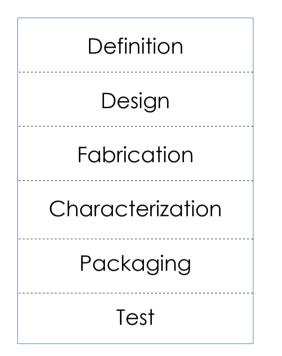
- Vertical vs. Horizontal / fabless business model
- Fabless model in photonic integration
- Fabless silicon photonics operation
- Design trends



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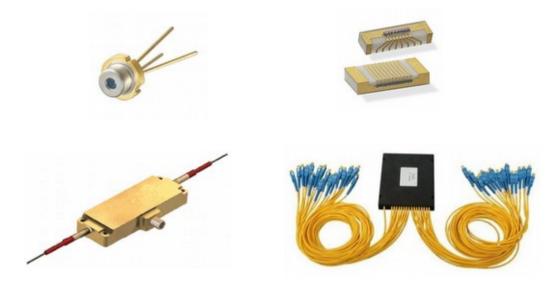


Vertical model

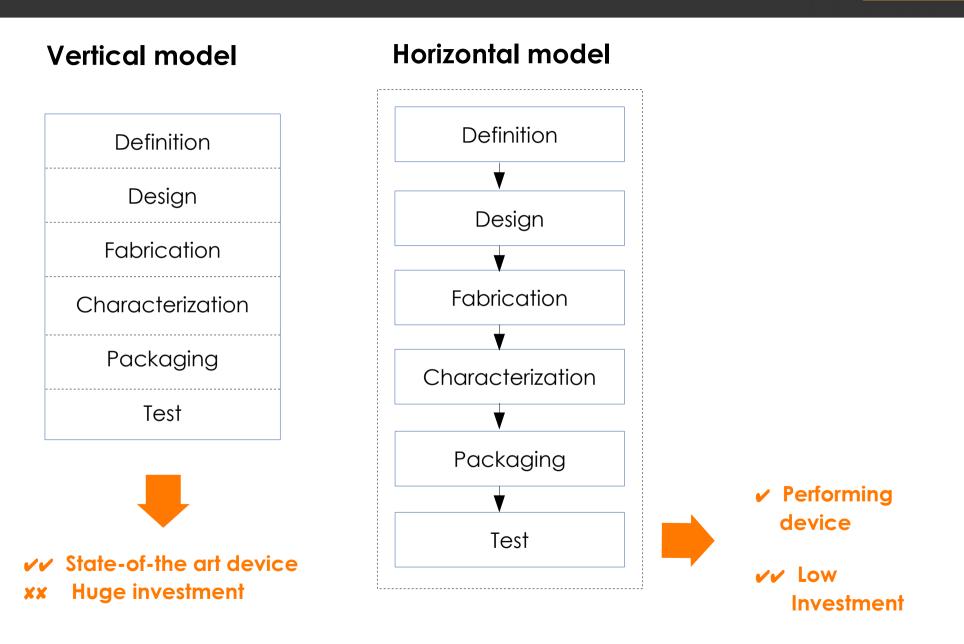


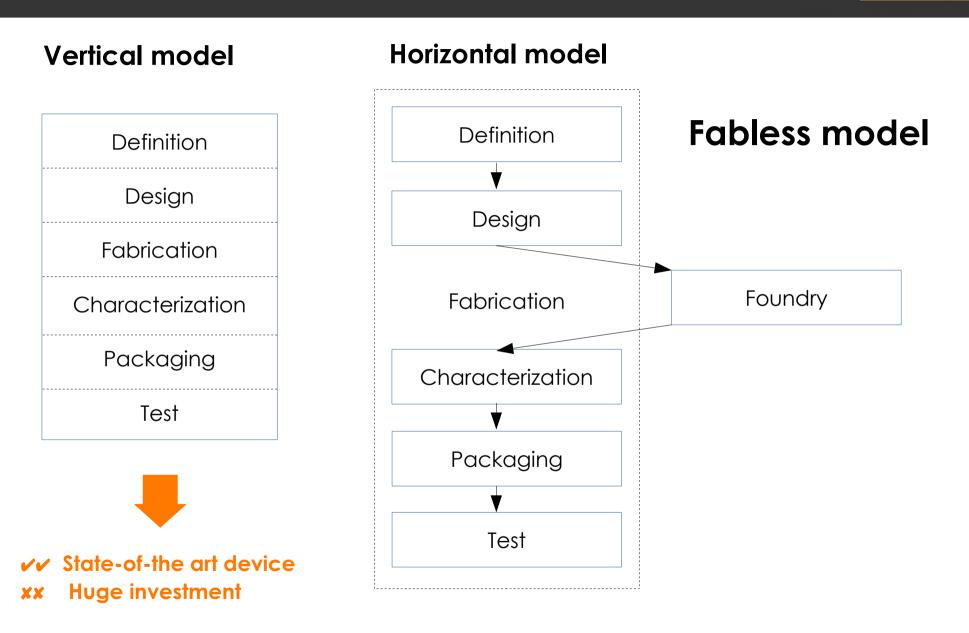


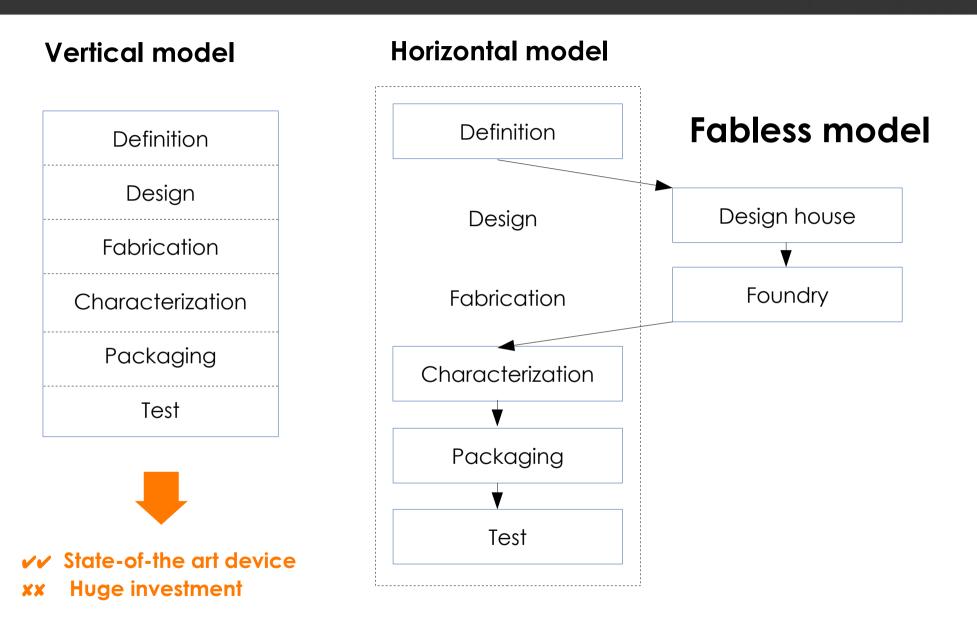
✓✓ State-of-the art device×× Huge investment

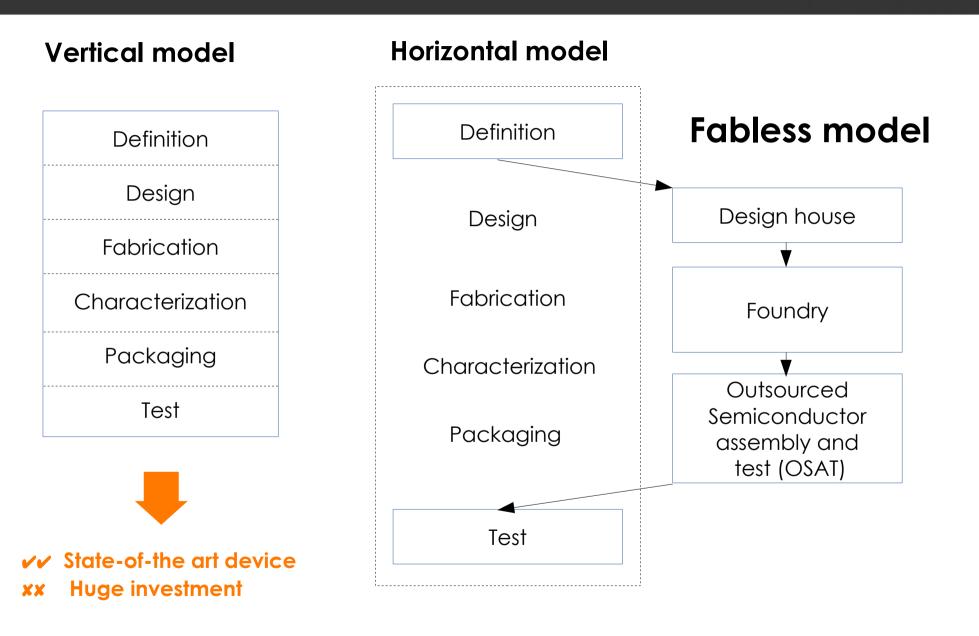


Traditional optical component manufacturers (lasers, PDs, splitters, AWGs, modulators, etc.)



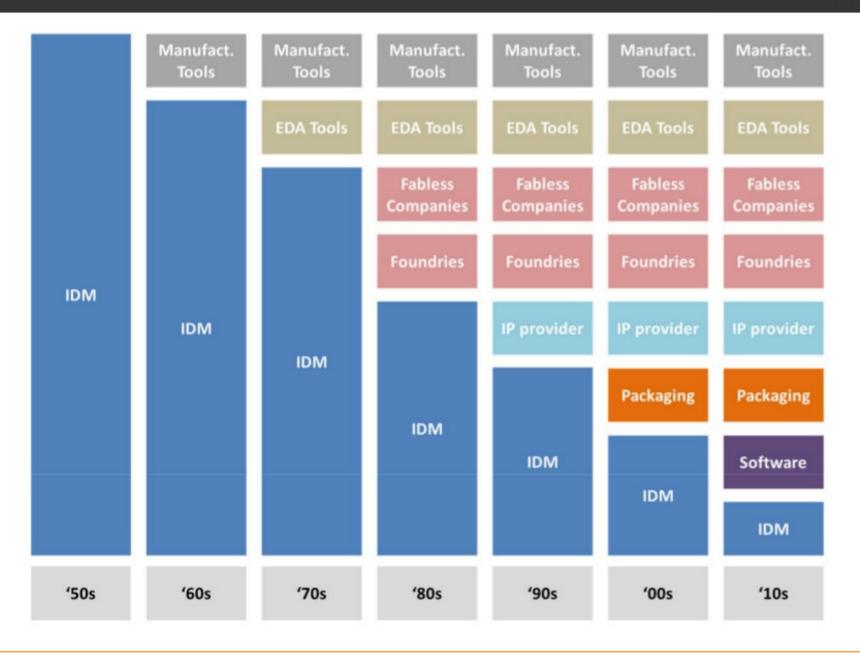




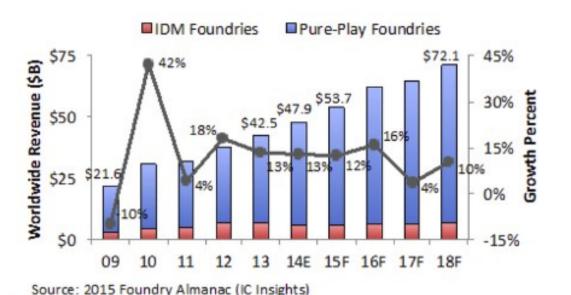


Horizontal business model





The growth of the fabless model



³⁰⁰ 263.€ Source: Statista 192.8 203.5 201 207.3 204.3203.9 186.1 193.6 200 173.9 171.8 150 100 50 2012 2013 2015 2010 2009 0h 2010 200 201 IDM IC sales Fabless/system company IC sales

In two decades...

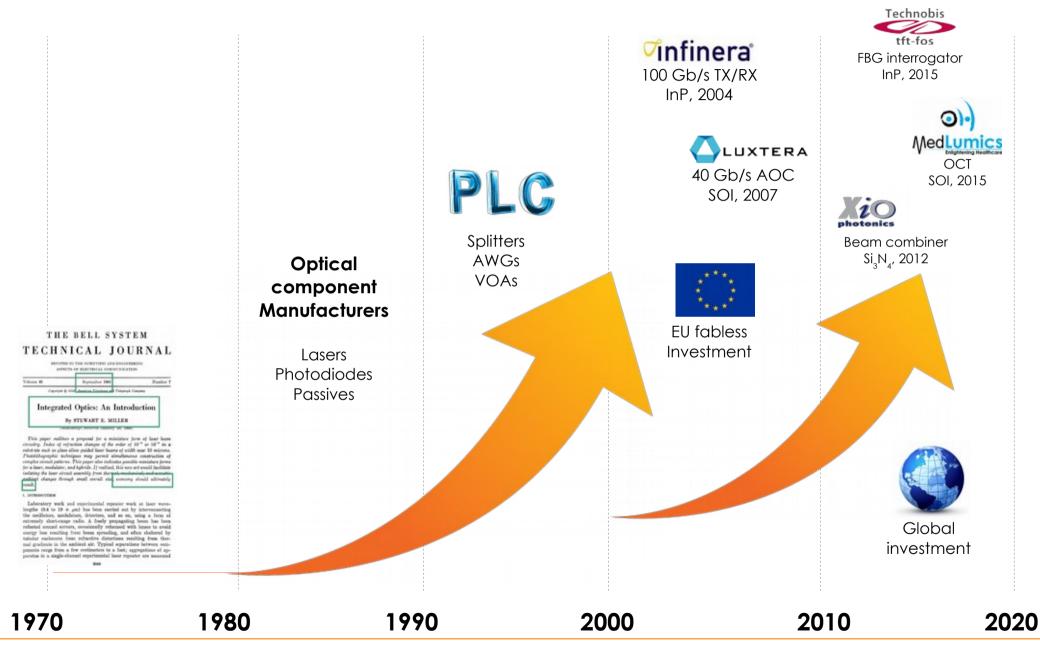
- Pure-play foundry revenues have grown, becoming the predominant manufacturing model.
- Wile IDM sales are still larger given the large concentration in few players, fabless sales have been growing faster and at a more stable rate over the last two decades.



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PIC technology evolution





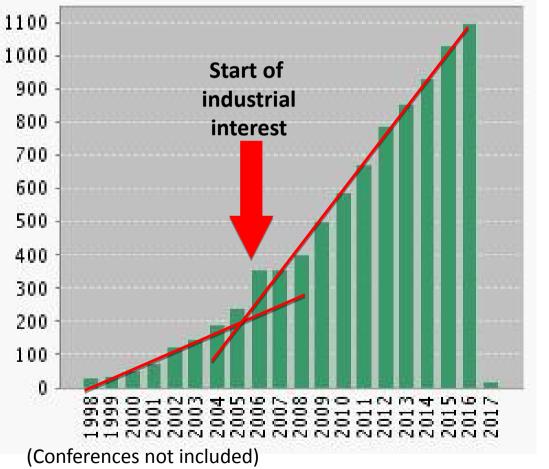
Silicon photonics technology take-up



Citation Report: 8566

(from Web of Science Core Collection)

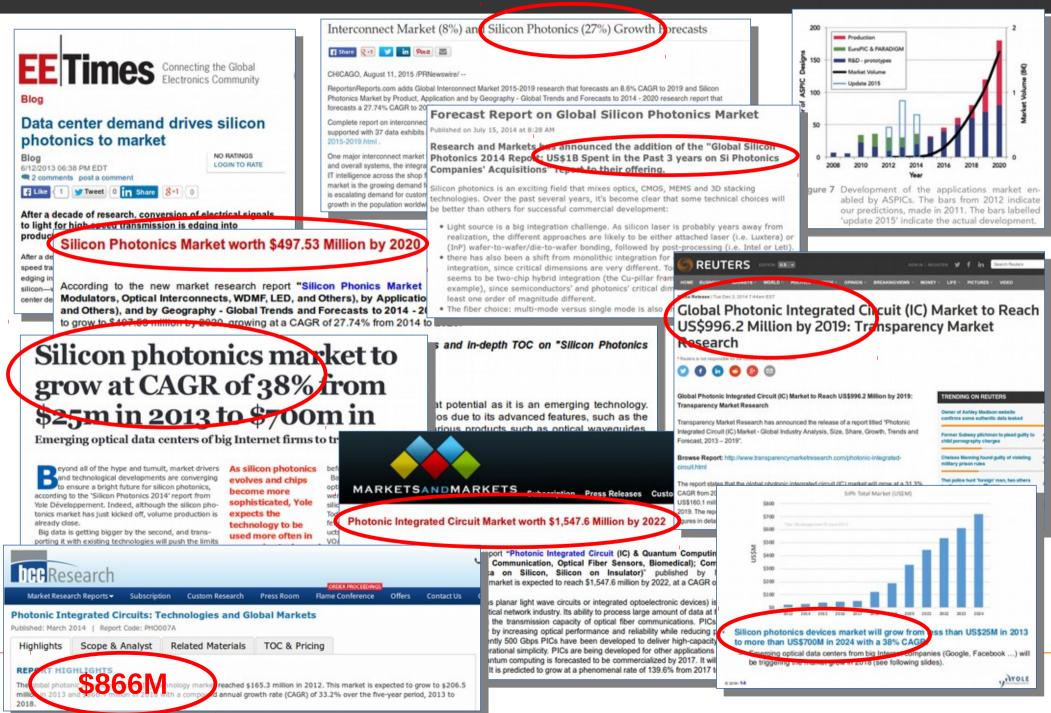
You searched for: TOPIC: (silicon) AND TOPIC: (photonic*) AND YEAR PUBLISHED: (1996-2017)



PUBLICATIONS EACH YEAR

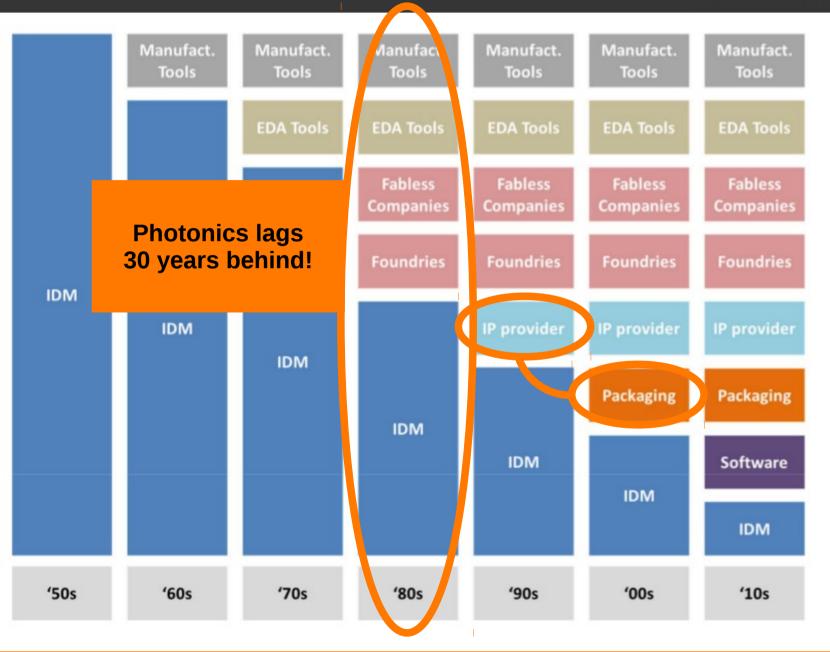
Courtesy Roel Baets, IMEC/UGhent

PIC market trends



Horizontal business model





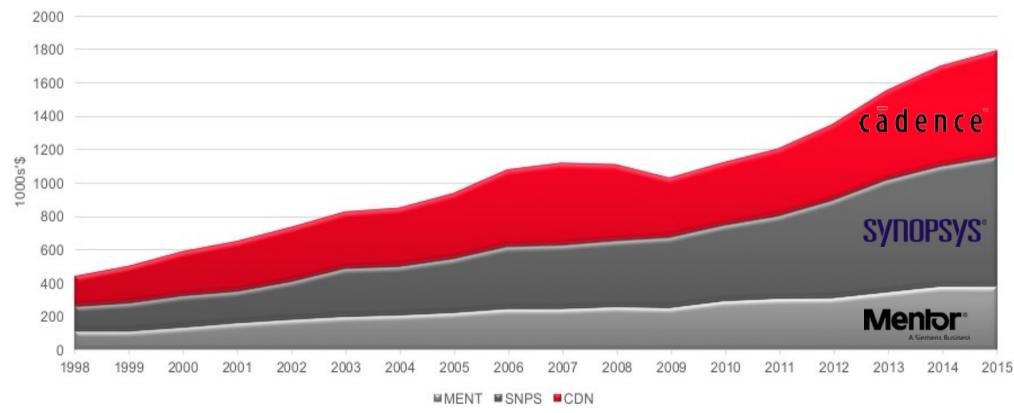


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Photonic EDA tools



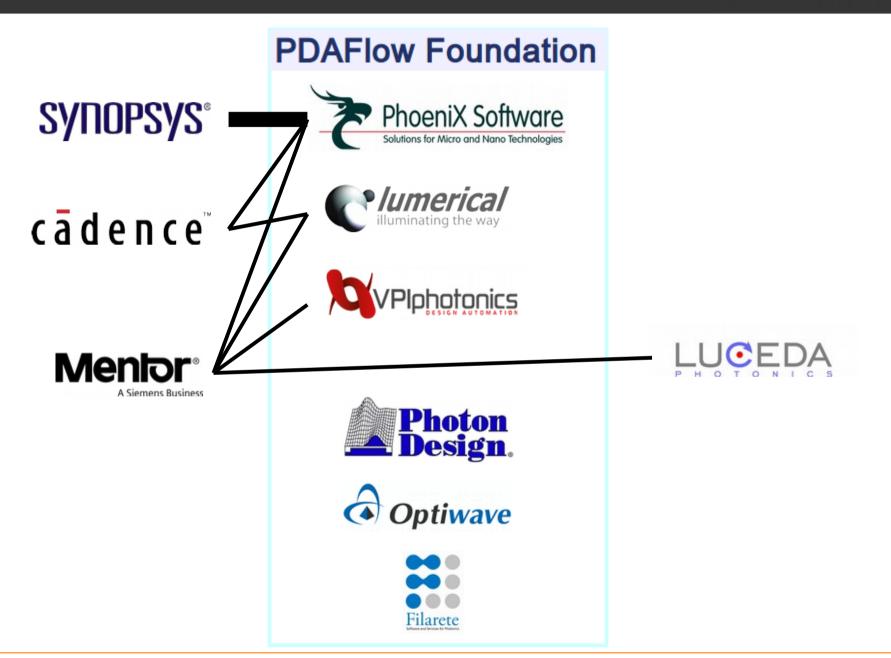
 Traditional Electronic Design Automation (EDA) tool vendors are heavily investing and partnering with smaller photonic design tool vendors.



Cumulative EDA R&D Spend

Photonic EDA tools (II)

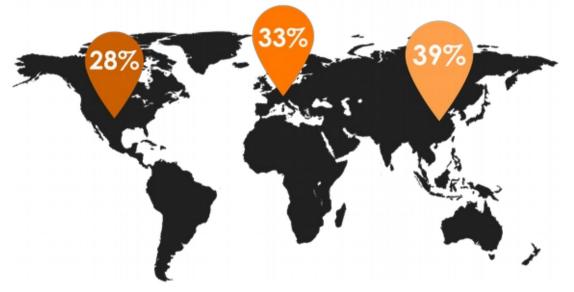




Fabless Si photonics manufacturing

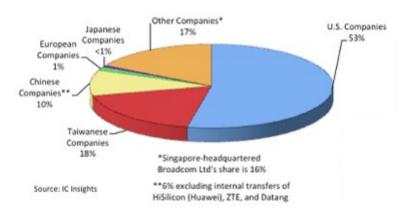


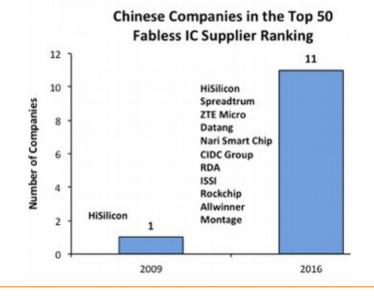
GEOGRAPHIC DISTRIBUTION OF SILICON PHOTONICS FOUNDRIES



- All major CMOS foundries investing, specially in Asia following IC trends.
- Proprietary generic processes: passives, actives (heaters, Ge PDs, Modulators, heterogeneous InP)
- Extra FEOL modules (SiN, SSC, etc.)
- BEOL options (Al/Cu, multilayer routing, TSV, pillars, etc.)
- Electronic-Photonic co-design

2016 Fabless Company IC Sales by Company Headquarters Location (\$90.4B)



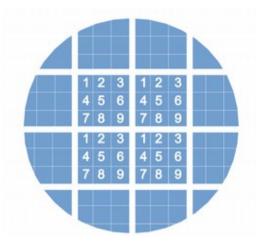


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Source: IC Insights

Fabless Si photonics manufacturing (II)

- Different software versions of Process Design Kits (PDKs) in place at most foundries, compiling design libraries with many mature building blocks for several processes.
- Multi-Project Wafer (MPW) runs available directly or through brokers for low-cost prototyping.
- R&D foundries setting up strategic agreements to transfer process and allow to scale-up production.





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VLC Photonics technical foundries report:

- 35 silicon photonic foundries, 6 brokers
- Contact info, capabilities, & PIC developments
- 180 pages & +650 references

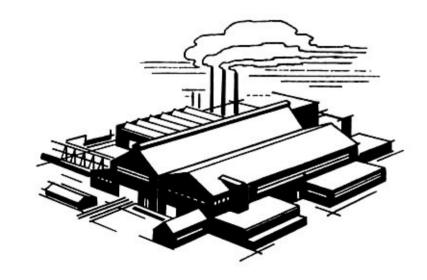


BUY ONLINE NOW

Challenges in fabrication



- Lack of updated information & roadmaps
- PDK availability & BB validation
- Turn around (cycle) time & delays
- Fabrication reporting
- Performance and delivery guarantees
- Wavelength range



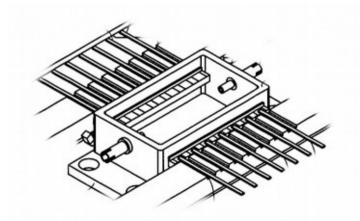
Test and Packaging

Back-end (post fab) processes comprise:

- Wafer metrology and probing
- Wafer back grinding (thinning) and dicing/cleaving
- Bare die characterization
- Packaging into component
- Component testing
- Assembly into module

Challenges in photonics still remain:

- High cost contribution at the back-end
- On wafer electrical+optical testing
- Package & assembly scalability
- Lack or fragmentation of standards
- DC+RF+optical package design & multiphysics
- Small pool of expertise and providers





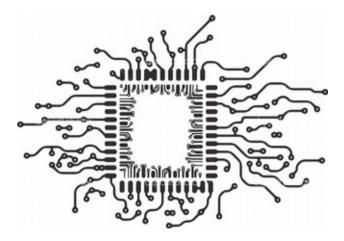


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PIC design challenges



- IP on building blocks / PDKs
- DRC validation & routing automatization
- Workflow standardization & tool interfacing
- Software licensing models and incumbent pricing
- Training & documentation
- Skilled workforce

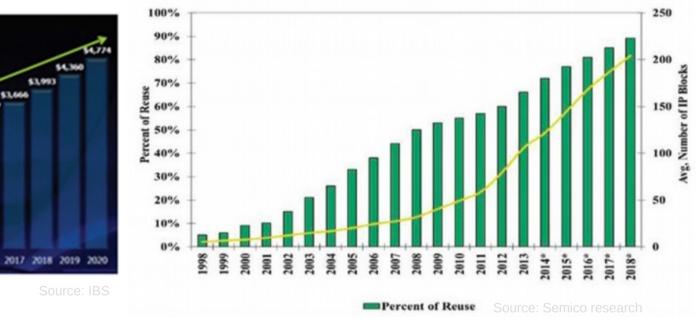


Design company trends

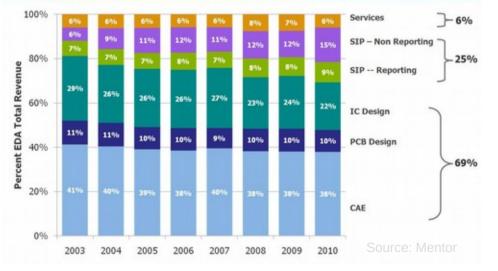


Company Type	Characteristics	Typical size
ID design consultants	1-2 person operation focusing on consulting on particular specialties	0.2 to 0.5M €
PIC design house	Always fabless, 3-25 people, sometimes also brokers fabrication or other services	0.5 to 2M €
IP / Technology licensing company	Usually focused on one technology or product area, engineering oriented management	2 to 15M €
Fabless chip firm	Growing fast to a niche product or market; usually fabless, strong marketing, product development and distribution departments, 20-200 people	< 200M €

IP approach in photonic integration







• Design IP is a large business in semiconductor markets.

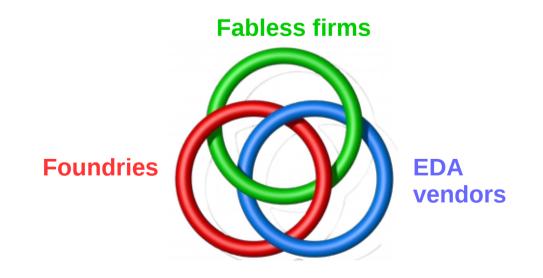
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- IP owned by:
 - Foundries
 - Fabless firms
 - EDA vendors

IP approach in photonic integration



- Photonics still lacks such business model, mainly due to:
 - Lack of market volume and enough licensee base,
 - Low maturity of fabrication processes, risky and expensive IP development,
 - IP usually limited to building blocks, not circuits,
 - Difficult IP usage, checking and enforcing,
 - Expensive patent/semiconductor topography registration, maintenance and defence, specially for SMEs.



Summary and take-aways



- Photonic integration is maturing very quickly due to growing market demands, and silicon photonics is profiting from all experience of the CMOS world.
- The fabless model is being successfully replicated in the photonic integration field.
- Main technical and business challenges remain on the backend processes.
- On the design side, the photonics EDA market is quickly consolidating, while design IP will take longer to become a market reality.

Thank you for your attention!



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